Fig-1

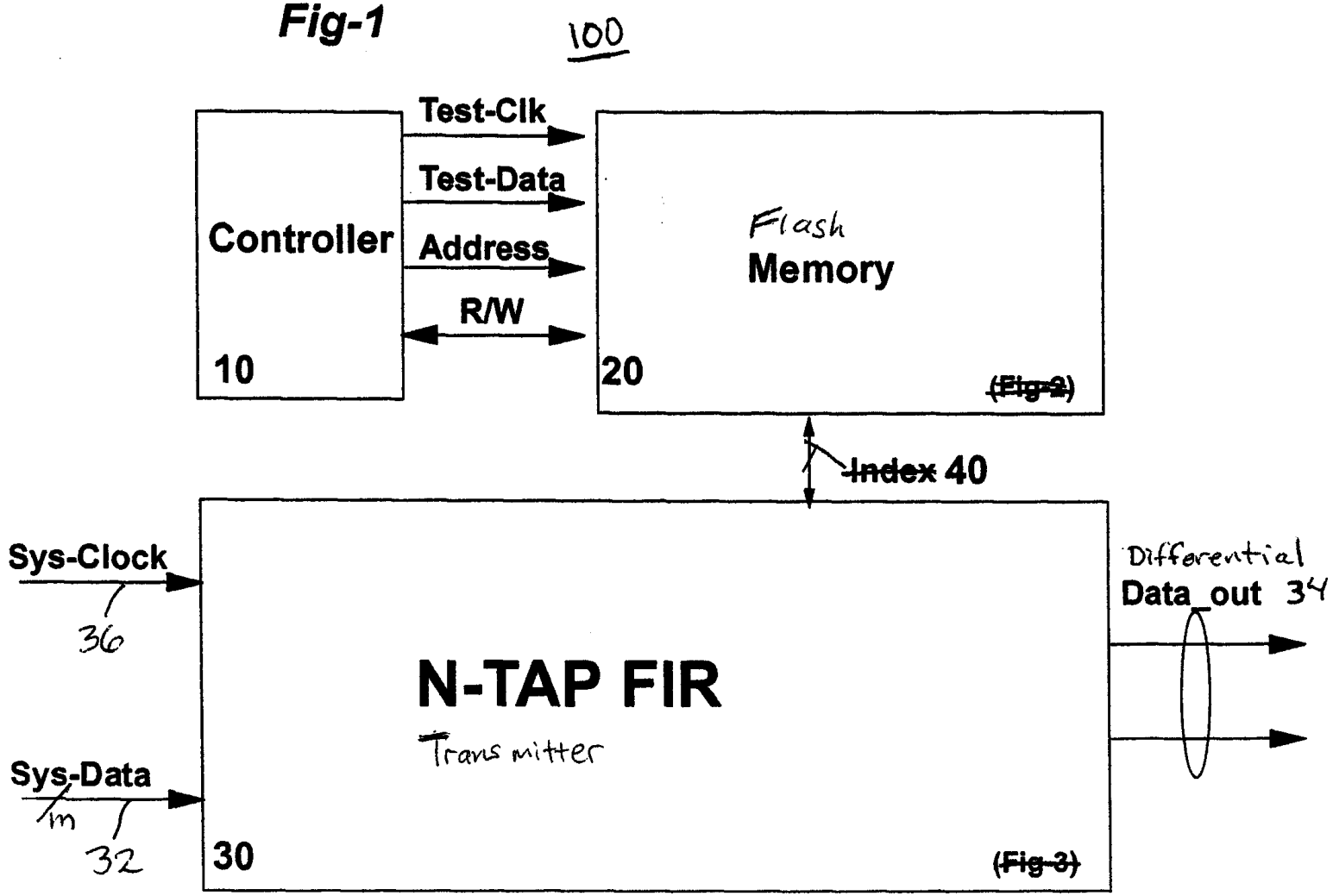

100
Test-Clk
Test-Data
Address
R/W
Controller
10
Flash
Memory
20
(Fig-2)
Index 40
Sys-Clock
36
Sys-Data
m
32
N-TAP FIR
Transmitter
30
(Fig-3)
Differential
Data_out 34

Fig-2

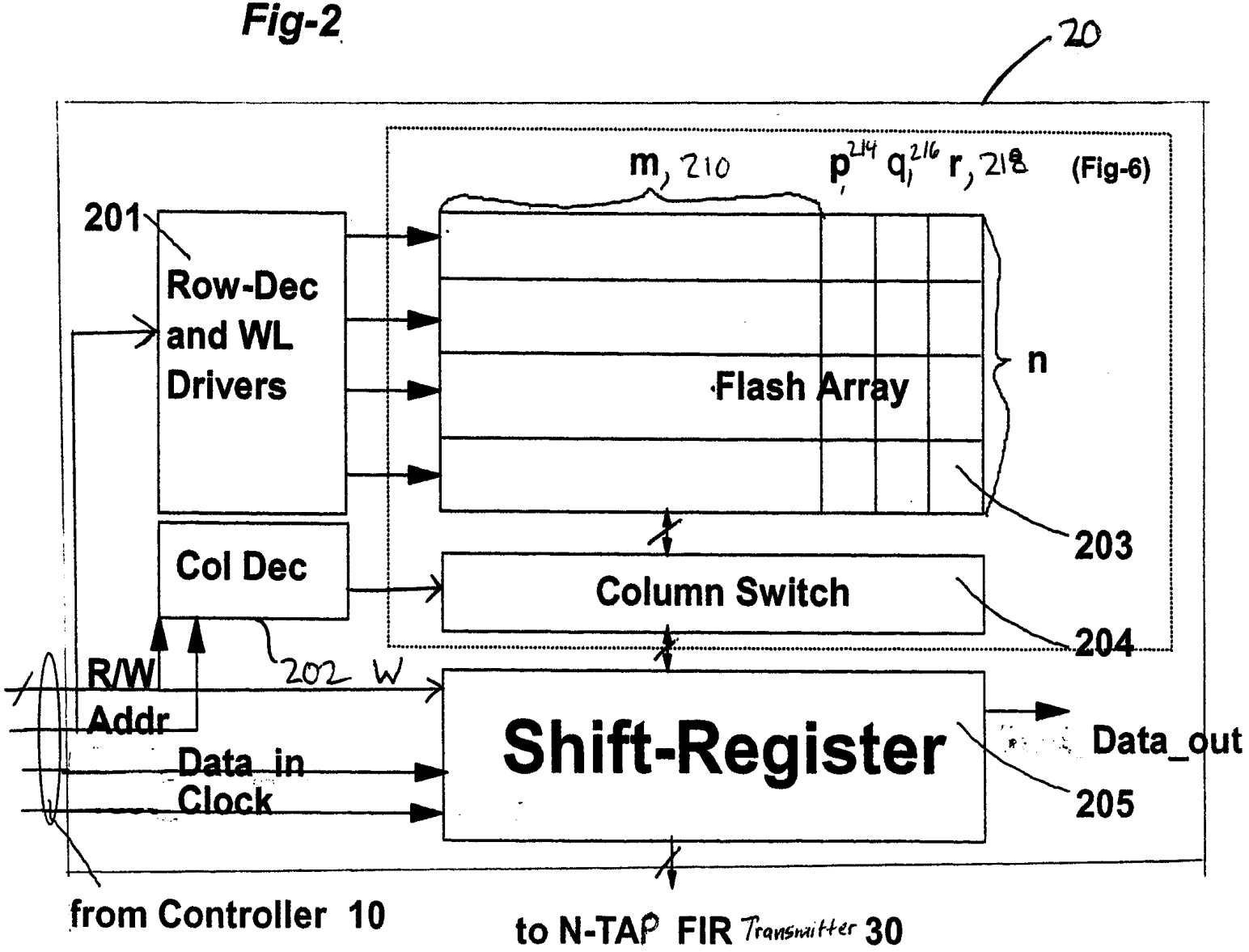

20
m, 210
p, 214
q, 216
r, 218
(Fig-6)
201
Row-Dec and WL Drivers
Flash Array
n
203
Col Dec
Column Switch
204
202 W
R/W
Addr
Data_in
Clock
Shift-Register
Data_out
205
from Controller 10
to N-TAP FIR Transmitter 30

Fig-3,

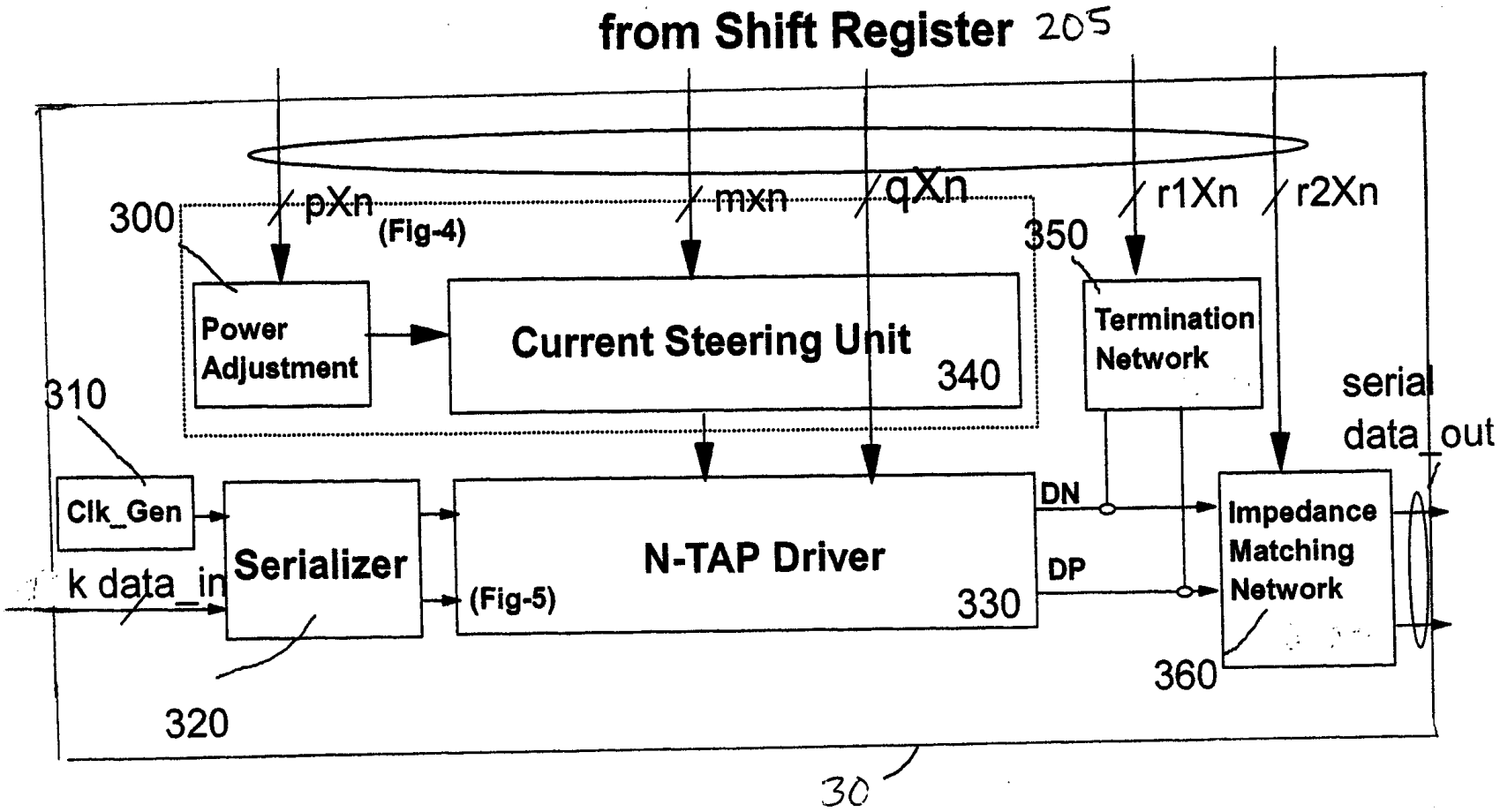

from Shift Register 205
300
pXn
(Fig-4)
mxn
qXn
r1Xn
r2Xn
350
Power Adjustment
Current Steering Unit
340
Termination Network
310
serial data_out
Clk_Gen
k data_in
Serializer
320
N-TAP Driver
(Fig-5)
330
DN
DP
Impedance Matching Network
360
30

Fig-4,

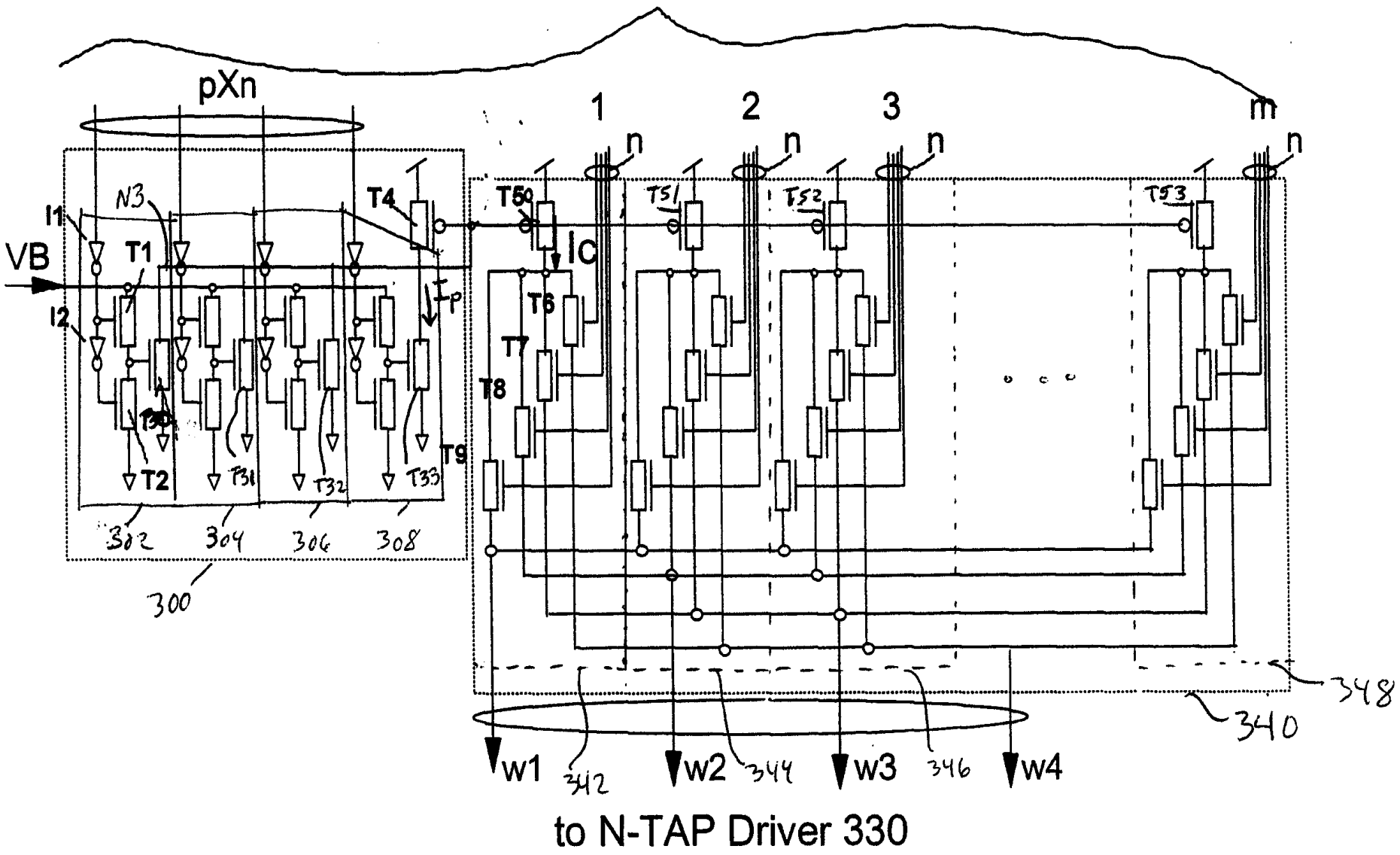

from Shift Register 205
pXn
1
2
3
m
n
N3
T4
T50
T51
T52
T53
I1
VB
T1
IC
I2
Ip
T6
T7
T8
T9
T2
T31
T32
T33
302
304
306
308
300
348
340
w1
342
w2
344
w3
346
w4
to N-TAP Driver 330

Fig-5

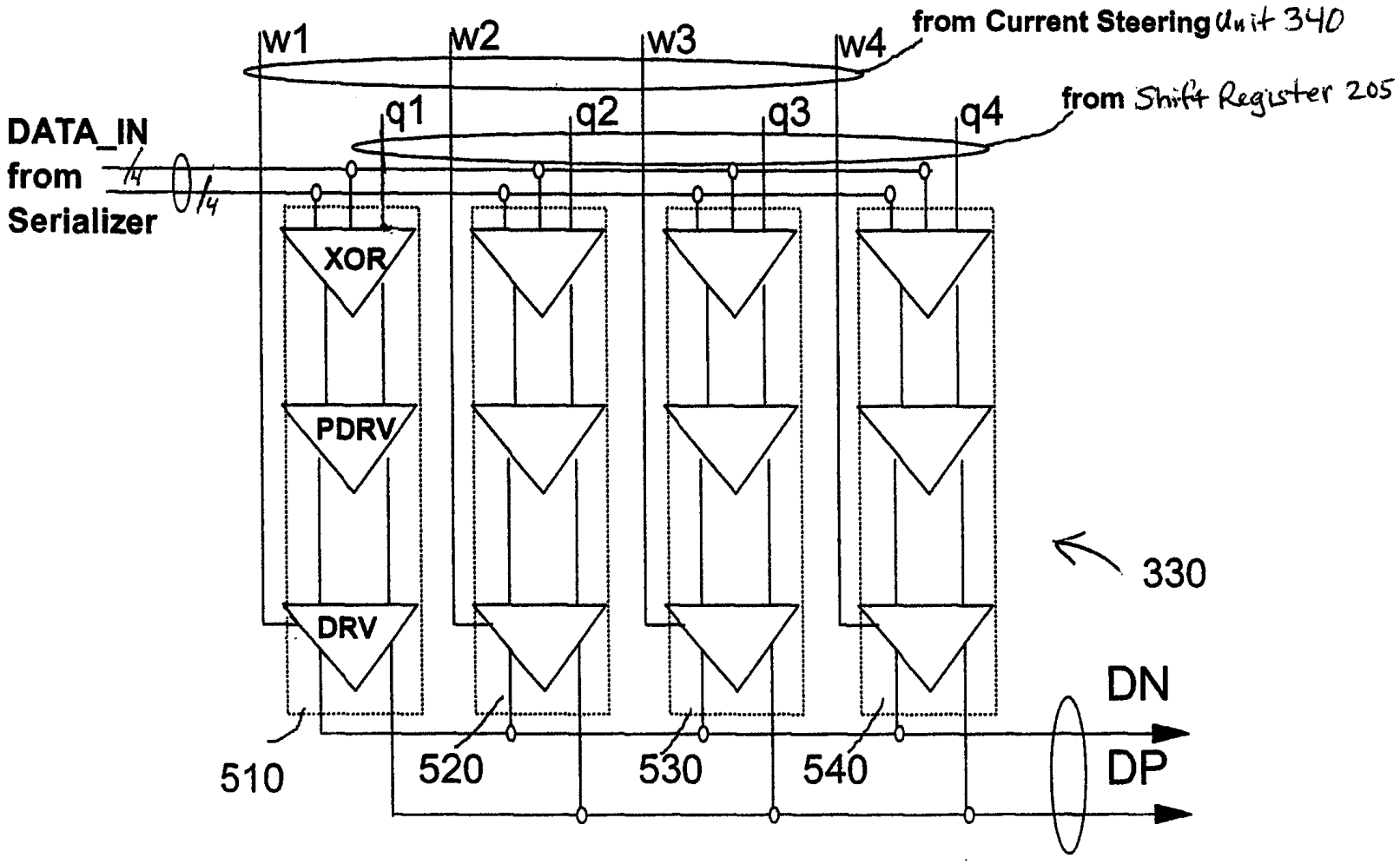

w1
w2
w3
w4
from Current Steering Unit 340
from Shift Register 205
q1
q2
q3
q4
DATA_IN
from
Serializer
4
4
XOR
PDRV
DRV
330
DN
DP
510
520
530
540

Fig-6

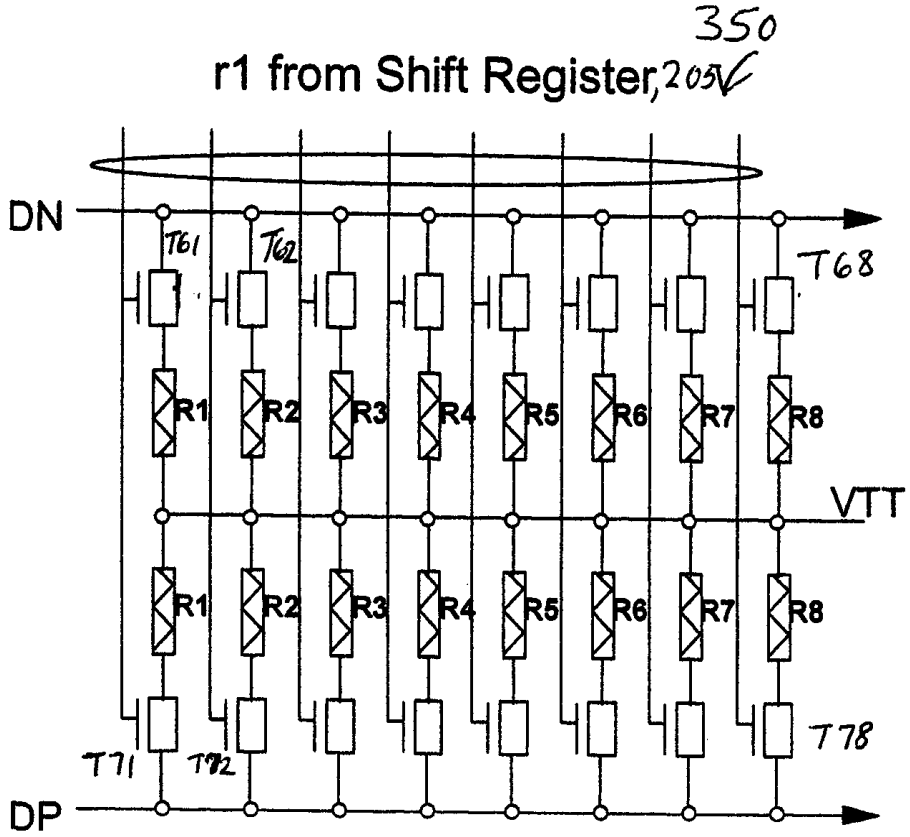
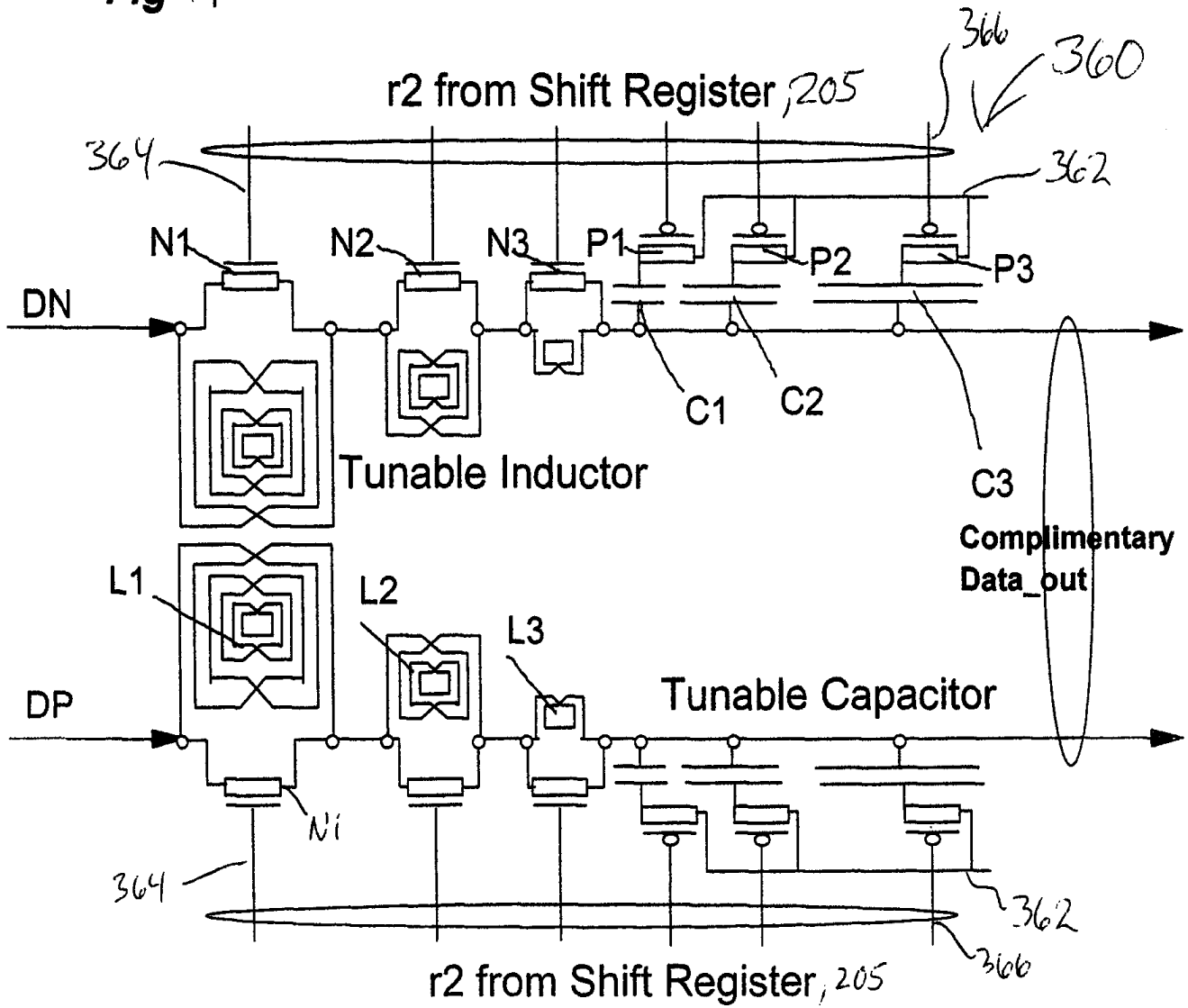

350
r1 from Shift Register, 205
DN
T61
T62
T68
R1
R2
R3
R4
R5
R6
R7
R8
VTT
R1
R2
R3
R4
R5
R6
R7
R8
T78
T71
T72
DP

Fig-7


r2 from Shift Register, 205
366
360
364
362
N1
N2
N3
P1
P2
P3
DN
C1
C2
C3
Tunable Inductor
Complimentary
Data_out
L1
L2
L3
DP
Tunable Capacitor
Ni
364
362
366
r2 from Shift Register, 205